a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Cont B3

23. (New) A semiconductor device as recited in claim 22, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

24. (New) A semiconductor device as recited in claim 22, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

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25. (New) A semiconductor device as recited in claim 22, wherein the plurality of supporting stubs further support the passivation layer.

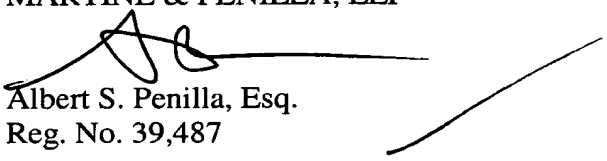
REMARKS

The Examiner is thanked for the careful review of this Application. In response to the Office Action, Restriction Requirement dated October 23, 2002, Applicants hereby elect, without traverse, Group I, claims 1-8 and 22-25, to prosecute in the above-identified Patent Application. Claims 1-8 and 22-25 are pending after entry of the present Amendment. Please add new claims 22-25 and cancel claim 21. Amendments were made to the claims to correct typographical errors and new claims were added in response to Examiner's Request for Restriction. These amendments do not introduce any new matter.

In view of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any additional

fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Atty. Docket: LAM2P246
Gotkis et al.	Examiner: H.K. Vu
Application No: 09/821,415	Group Art Unit: 2811
Filed: March 28, 2001	Date: November 22, 2002
For: SEMICONDUCTOR STRUCTURE IMPLEMENTING LOW-K DIELECTRIC MATERIALS AND SUPPORTING STUBS (As Amended)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on November 22, 2002.

Signed: _____
Kay Harlow

MARKED-UP CLAIMS

3. **(Amended)** A semiconductor device as recited in claim 1, wherein the plurality of supporting stubs **[are]** **is** not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

7. **(Amended)** A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs **[are]** **is** not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

22. (New) A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias isolated from each other by an air dielectric; and

a plurality of filled supporting stubs, each of the plurality of filled supporting stubs formed from a same contiguous material, each of the plurality of supporting stubs further configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device;

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

23. (New) A semiconductor device as recited in claim 22, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

24. (New) A semiconductor device as recited in claim 22, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

25. (New) A semiconductor device as recited in claim 22, wherein the plurality f supporting stubs further support the passivation layer.